	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Inventor
1	US 6214667 B1	20010410	9	Method for fabricating a flash memory	438/257	438/594	Ding, Yen-Lin et al.
2	US 5982017 A	19991109	5	Recessed structure for shallow trench isolation and salicide processes	257/513	257/374; 257/510; 257/515; 257/754	Wu, Sheng-Jyh et al.
3	US 5891771 A	19990406	7	Recessed structure for shallow trench isolation and salicide process	438/248	438/246; 438/247; 438/301; 438/303; 438/305; 438/424; 438/427; 438/700; 438/701	Wu, Sheng-Jyh et al.
4	US 6184571 B1	20010206	11	Method and apparatus for endpointing planarization of a microelectronic substrate	257/635	257/915; 438/634	Moore, John T.
5	US 6159821 A	20001212	9	Methods for shallow trench isolation	438/424	438/296; 438/427	Cheng, Hsu-Li et al.
6	US 6146970 A	20001114	17	Capped shallow trench isolation and method of formation	438/424	438/294; 438/295; 438/296; 438/318; 438/353; 438/355; 438/359	Witek, Keith E. et al.
7	US 6091129 A	20000718	44	Self-aligned trench isolated structure	257/510	257/622; 438/296	Cleeves, James M.
8	US 6057580 A	20000502	26	Semiconductor memory device having shallow trench isolation structure	257/396	257/397; 257/513	Watanabe, Hiroshi et al.

Plus

PLUS Search Results for S/N 10/056,179, Searched June 13, 2002 (Top 50)

6001687	5516625	6184571	6002160	6146970
5879980	6057580	4763177	6031269	6159821
5891771	6140688	5380676	6049107	6184107
5982017	6225171	5572056	6074927	6222224
6071779	6225171	5691215	6091129	6222224
6121078	4969022	5710076	6093947	4593459
6177299	5492858	5830797	6093619	4633290
6214667	5908311	5837612	6133116	4801988
6214667	5976982	5937297	6133113	4894697
6294817	6054343	5936280	6136663	4920065

Most Frequently Occurring Classifications of Patents Returned
From A Search of 10/056,179 on June 13, 2002

Combined Classifications
11 438/424
10 438/296
7 438/427
5 257/510
5 438/221
4 257/513
4 257/515
3 257/315
3 257/347
3 257/374
3 257/402
3 438/257
3 438/305
3 438/404
3 438/430
3 438/435
2 148/DIG 50
2 257/302
2 257/304
2 257/321
2 257/333
2 257/397
2 257/506
2 257/622
2 438/238
2 438/243
2 438/244
2 438/297
2 438/301
2 438/359
2 438/400
2 438/425
2 438/437
2 438/594
2 438/692
2 438/699
2 438/706
2 438/778

11 438/424 (4 OR, 7 XR)
Class 438 : SEMICONDUCTOR DEVICE MANUFACTURING: PROCESS

438/400 FORMATION OF ELECTRICALLY ISOLATED LATERAL SEMICONDUCTIVE STRUCTURE
438/424 .Grooved and refilled with deposited dielectric material

10 438/296 (3 OR, 7 XR)
Class 438 : SEMICONDUCTOR DEVICE MANUFACTURING: PROCESS

438/142 MAKING FIELD EFFECT DEVICE HAVING PAIR OF ACTIVE REGIONS SEPARATED BY GATE STRUCTURE BY FORMATION OR ALTERATION OF SEMICONDUCTIVE ACTIVE REGIONS
438/197 .Having insulated gate (e.g., IGFET, MISFET, MOSFET, etc.)
438/294 ..Including isolation structure
438/296 ...Dielectric isolation formed by grooving and refilling with dielectric material

7 438/427 (1 OR, 6 XR)
Class 438 : SEMICONDUCTOR DEVICE MANUFACTURING: PROCESS

438/400 FORMATION OF ELECTRICALLY ISOLATED LATERAL SEMICONDUCTIVE STRUCTURE
438/424 .Grooved and refilled with deposited dielectric material
438/427 ..Refilling multiple grooves of different widths or depths

5 257/510 (1 OR, 4 XR)
Class 257 : ACTIVE SOLID-STATE DEVICES
257/499 INTEGRATED CIRCUIT STRUCTURE WITH ELECTRICALLY ISOLATED COMPONENTS
257/506 .Including dielectric isolation means
257/509 ..Combined with pn junction isolation (e.g., isoplanar, LOCOS)
257/510 ...Dielectric in groove

5 438/221 (1 OR, 4 XR)
Class 438 : SEMICONDUCTOR DEVICE MANUFACTURING: PROCESS

438/142 MAKING FIELD EFFECT DEVICE HAVING PAIR OF ACTIVE REGIONS SEPARATED BY GATE STRUCTURE BY FORMATION OR ALTERATION OF SEMICONDUCTIVE ACTIVE REGIONS
438/197 .Having insulated gate (e.g., IGFET, MISFET, MOSFET, etc.)
438/199 ..Complementary insulated gate field effect transistors (i.e., CMOS)
438/218 ...Including isolation structure
438/221 ....Dielectric isolation formed by grooving and refilling with dielectric material

4 257/513 (2 OR, 2 XR)
Class 257 : ACTIVE SOLID-STATE DEVICES
257/499 INTEGRATED CIRCUIT STRUCTURE WITH ELECTRICALLY ISOLATED COMPONENTS
257/506 .Including dielectric isolation means
257/509 ..Combined with pn junction isolation (e.g., isoplanar, LOCOS)
257/510 ...Dielectric in groove
257/513 ....Vertical walled groove

4 257/515 (0 OR, 4 XR)

Class 257 : ACTIVE SOLID-STATE DEVICES
257/499 INTEGRATED CIRCUIT STRUCTURE WITH ELECTRICALLY ISOLATED COMPONENTS
257/506 .Including dielectric isolation means
257/509 ..Combined with pn junction isolation (e.g., isoplanar, LOCOS)
257/510 ...Dielectric in groove
257/515 ....With active junction abutting groove (e.g., "walled emitter")

3 257/315 (3 OR, 0 XR)
Class 257 : ACTIVE SOLID-STATE DEVICES
257/213 FIELD EFFECT DEVICE
257/288 .Having insulated electrode (e.g., MOSFET, MOS diode)
257/314 ..Variable threshold (e.g., floating gate memory device)
257/315 ...With floating gate electrode

3 257/347 (2 OR, 1 XR)
Class 257 : ACTIVE SOLID-STATE DEVICES
257/213 FIELD EFFECT DEVICE
257/288 .Having insulated electrode (e.g., MOSFET, MOS diode)
257/347 ..Single crystal semiconductor layer on insulating substrate (SOI)

3 257/374 (1 OR, 2 XR)
Class 257 : ACTIVE SOLID-STATE DEVICES
257/213 FIELD EFFECT DEVICE
257/288 .Having insulated electrode (e.g., MOSFET, MOS diode)
257/368 ..Insulated gate field effect transistor in integrated circuit
257/369 ...Complementary insulated gate field effect transistors
257/373 ....With pn junction to collect injected minority carriers to prevent parasitic bipolar transistor action
257/374 .....Dielectric isolation means (e.g., dielectric layer in vertical grooves)

3 257/402 (1 OR, 2 XR)
Class 257 : ACTIVE SOLID-STATE DEVICES
257/213 FIELD EFFECT DEVICE
257/288 .Having insulated electrode (e.g., MOSFET, MOS diode)
257/402 ..With permanent threshold adjustment (e.g., depletion mode)

3 438/257 (3 OR, 0 XR)
Class 438 : SEMICONDUCTOR DEVICE MANUFACTURING: PROCESS

438/142 MAKING FIELD EFFECT DEVICE HAVING PAIR OF ACTIVE REGIONS SEPARATED BY GATE STRUCTURE BY FORMATION OR ALTERATION OF SEMICONDUCTIVE ACTIVE REGIONS

	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Inventor
1	US 20020033517 A1	20020321	11	Non-volatile semiconductor memory device	257/510	257/202; 257/314; 257/315	Lojek, Bohumil
2	US 20020005561 A1	20020117	25	NON-VOLATILE SEMICONDUCTOR MEMORY DEVICE AND MANUFACTURING METHOD THEREOF	257/510		KOBAYASHI, KIYOTERU et al.
3	US 6376877 B1	20020423	12	Double self-aligning shallow trench isolation semiconductor and manufacturing method therefor	257/317	257/315; 257/321; 257/510	Yu, Allen S. et al.
4	US 6281103 B1	20010828	13	Method for fabricating gate semiconductor	438/593	438/296	Doan, Trung Tri
5	US 6271561 B1	20010807	11	Method for fabricating floating gate semiconductor devices with trench isolation structures and self aligned floating gates	257/316	257/510	Doan, Trung Tri
6	US 6222225 B1	20010424	20	Semiconductor device and manufacturing method thereof	257/315	257/374; 257/506; 257/510	Nakamura, Takuya et al.
7	US 6107670 A	20000822	19	Contact structure of semiconductor device	257/510	257/315; 257/640; 257/760	Masuda, Kazunori
8	US 6034393 A	20000307	31	Nonvolatile semiconductor memory device using trench isolation and manufacturing method thereof	257/315	257/321; 257/506; 257/510	Sakamoto, Osamu et al.
9	US 5051795 A	19910924	15	EEPROM with trench-isolated bitlines	257/317	257/321; 257/510	Gill, Manzur et al.

257/510 +FG